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International Journal of VLSI design & Communication Systems (VLSICS) Vol2, No4, December 2011 SRAM CELL BASED ON CNTFET AT 32nm TECHNOLOGY Rajendra Prasad S 1, Prof B K Madhavi 2 and Prof K Lal Kishore 3 1Department of ECE, ACE Engineering College, Hyderabad, AP, India srprasad447@gmailcom 2Department of ECE, GCET, Keesara, Hyderabad

A 80Ms/sec 10bit PIPELINED ADC Using 1.5Bit Stages And ...

PPrasad Rao 1 and ProfKLal Kishore 2, 1 Research Scholar, JNTU-Hyderabad prasadrao_hod@yahoocoin 2Director, R&D, JNTU-Hyderabad lalkishorek@yahoocom Abstract Use of pipelined ADCs is becoming increasingly popular both as stand alone parts and as embedded functional units in SOC design

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