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8. UART Core

Altera Corporation 8-1 May 2007 8 UART Core Core Overview The universal asynchronous receiver/transmitter core with Avalon® interface (UART core) implements a method to communicate serial character streams between an embedded system on an Altera ...

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5. JTAG UART Core with Avalon Interface

The JTAG UART core uses the JTAG circuitry built in to Altera FPGAs, and provides host access via the JTAG pins on the FPGA The host PC can connect to the FPGA via any Altera JTAG download cable, such as the USB-Blaster™ cable Software support for the JTAG UART core is provided by Altera...

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Core Version This handbook applies to CoreUART v56 The release notes provided with the core list known discrepancies between this handbook and the core release associated with the release notes Figure 1 • System Block Diagram Depicting CoreUART Usage UART Microsemi Device Industry Standard UART ...