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40 Estimating FPGA Power Consumption 233 41 Pin Assignment 238 42 Thermal Analysis 242 43 FPGA Cost Estimate 247 44 GPGPU vs FPGA 250 45 ASIC to FPGA Migration tasks 253 46 Differences Between ASIC and FPGA Designs 258 47 Selecting ASIC Emulation or Prototyping Platform 261 48 Partitioning an ASIC design into multiple FPGAs 269 49

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Irrespective of the FPGA being used, the end system dictates the power supply challenges. For example, in a DVD recorder with satellite broadcast, dozens of power rails may be required in addition to powering the FPGA. In such a system, power supply size and efficiency may not be a premium, but very low cost is. Conversely, in battery-operated

Implementing Single-Chip FPGA Power Solutions

POWER designer Implementing Single-Chip FPGA Power Solutions The simplified diagram in Figure 3 shows the implementation of a three-rail, higher power FPGA supply. In this case, an LM2633 controller is providing 10V to a Xilinx Virtex 5 core, 33V to the I/Os and 25V for VCCAUX. The LM2633 is a triple output IC, and is a perfect example of

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Current (mA) 1 10 100 1000 100 90 80 70 60 50 40 30 20 10 0 V OUT

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Total on-chip power is the power consumed internally within the FPGA, equal to the sum of device static power and design power. It is also known as thermal power. Off-Chip Power Off-chip power is the current that flows from the supply source through the FPGA power pins, then out of the I/Os and dissipated in external board components. The currents

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The embedded logic analyzer is typically implemented using FPGA fabric and is inserted into the design. The JTAG port is used to access the analyzer and the captured data can be displayed on a PC. When external test equipment is used, the FPGA design under test is modified so that selected internal FPGA signals are routed to output pins.

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1 Connect the USB cable coming together with the Cyclone 10 LP FPGA Evaluation Kit between the PC and the kit as shown in Figure 1 2 The USB cable will supply the power as well as establish the JTAG connection with the kit 3 To enable RSU feature, make sure SW14 set to 1 (move to left side from the view of Figure 1)

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